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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,429	11/03/2003	Glenn Joseph Leedy	ELM-1 Cont. 10	5639
1473	7590	04/05/2006	EXAMINER	
FISH & NEAVE IP GROUP ROPE & GRAY LLP 1251 AVENUE OF THE AMERICAS FL C3 NEW YORK, NY 10020-1105			RAO, SHRINIVAS H	
			ART UNIT	PAPER NUMBER
			2814	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/700,429	LEEDY, GLENN JOSEPH	
	Examiner Steven H. Rao	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 20 January 2006.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 77-272 is/are pending in the application.
- 4a) Of the above claim(s) 77-109, 211-222 and 254-272 is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 110-2209 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All    b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____
3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date <u>4/27; 1/24; 4/11; 7/05; 1/11; 7/12; 10/09/09</u>	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____

***Response to Amendment***

Applicants' amendment filed on Jan 11, 2006 has been entered and forwarded to the examiner on Jan. 20, 2006.

Therefore claims 109,118,122,131,135,144,163,170,179,186,195 and 202 as amended by the amendment ( subject to the new matter rejection below and not entered ) and claims 110-117,119-121,123-130,132-134,136-143,145-162,164-169,171-178,180-185,187-194,196-201 and 202-210 and 223-258 as previously recited are currently pending in the Application.

Claims 77-108 and 211-222 were previously withdrawn from consideration.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 109,122,135,163,179 and 195 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

All the above claims recite, " forming on the substrate circuitry including a plurality of integrated circuits having active devices, at least one of the integrated circuits having a uniform thickness throughout a full extent thereof " the presently newly added limitation at least one of the integrated circuits having a uniform thickness

throughout a full extent thereof was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

It is noted that the specification describes various sub elements like semiconductor substrate (para 0014) , membrane ( 0017, 0077, 0078,0092, 0099, 0223) none of these or any where in the specification is there is disclosure/description of at least one of the integrated circuits having a uniform thickness throughout a full extent thereof.

Therefore independent claims 109,122,135,163,179 and 195 ( and dependent claims 110-121, 123-134, 136-162, 164-178,180-194, 196-210 and 223-258 at least for depending from rejected claims ) are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement claims .

Appropriate correction is required.

#### ***Claim Rejections - 35 USC Section 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action'.

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pedains.

Patentability shall not be negated by the manner in which the invention was

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made.

Claims 109-201 and 223-258 are rejected under 35 U.S.C. 103 as being unpatentable over Shimoji ( U.S. Patent No. 5,420,458, herein after Shimoji) and Mattox ( U.S. Patent No. 4,825,277, herein after Mattox).

With respect to claim 109, 122 , 163, 179 and 194, Shimoji describes a method of making an integrated circuit including the steps of : Forming a thin substrate ( Shimoji, Fig. 3 A # 21, col. 3 line 48) and forming on the substrate circuitry including active devices ( Shimoji, Fig. 2 C # 51, 52, col. 3 lines 65-68) ;

The presently newly added limitation " at least one of the integrated circuits having a uniform thickness throughout a full extent thereof" is new matter and therefore not given patentable weight..

Shimoji does nor specifically describe the integrated circuit is substantially flexible while retaining its structural integrity.

However Mattox in col. 9 lines 1-13 describes the integrated circuit is substantially flexible while retaining its structural integrity to the semiconductor surface.

Therefore it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the Mattox's stress controlled dielectric membrane instead of Shimoji's to dielectric layer form devices having controlled stress relative to the semiconductor surface (Mattox col. 2 lines 5-10).

And removing a major portion of the semiconductor substrate while retaining the structural integrity ( Shimoji Fig. 6 B # 8, col. 4 lines 50-57).

With respect to dependent claims 1 10- 114, 123-127, 136-140, 147-150, 153-155, 159-160,164-166,174-176,180-182,190-192, 196-198 and 206-209 , wherein the thin substrate is formed prior to forming circuitry ( Shimoji, Fig. 3 A # 21, col. 3 line 48),, after forming said circuitry, (Shimoji fig. 4 , col. 4 lines 5-15) an elastic dielectric layer overlying the active devices. ( Shimoji, Fig. 2 C # 51, 52, col. 3 lines 65-68, Mattox) ; deposition of elastic dielectric film by RF , CVD, PECVD ( Mattox , all well known in the art methods of deposition and also Shimoji col. 4 lines 15-20).

With respect to dependent claims 115, 128, 141, 151,156,161,167,177, 183; 193, 8 2 199 , wherein the dielectric membrane is caused to have a stress of  $8 \times 10$  dynes/cm or less. ( See Mattox claim 9 and Mattox does not specifically mention a surface stress f  $8 \times 10^8$  dynes/cm 2. However Mattox in col. 7 lines 45-52 describes the stress range to be between -1 to  $5 \times 10^8$  dynes/cms to  $1 \times 10^9$  to form devices having controlled stress relative to the semiconductor surface ).

Therefore it would have been obvious to a person of ordinary skill in the art at the time of the invention to use the stress range  $8 \times 10^8$  dynes/cm 2 instead of Mattox's 9 dynes/cm<sup>2</sup> to  $1 \times 10^9$  dynes/cm previously described overlapping range of 1 to  $5 \times 10^8$  to form devices having controlled stress relative to the semiconductor surface (Mattox col. 2 lines 5-10).

With respect to claims 1 16, 1 19 -120, 129, 132-133, 142, 145-146, 149, 157-159 162-164-165, 168, 171-172,174, 178, 184,187-188, 194, 196-197, 200, 203-204, 206-207 and 210 wherein the stress is tensile (Mattox abstract line 8, etc., silicon or dielectric substrate ( Shmioji see rejection of clam 110 above) ;

With respect to remaining claims including claims 117-118, 130-131, 134-135, 141, 143-144, 145, 156, 167-170, 177, 183, 185-186, 193, 195, 199, 201-202, 206-209 and Claims 121, 147 and 205 wherein the integrated circuit can be thinned to 50 microns. (Mattox col. 4 lines 15-23). and 205 wherein the dielectric layer is formed of inorganic material of an oxide of silicon, a nitride of silicon (Shimoji, silicon dioxide/nitride) or organic (Shimoji or well known - e.g. TOES).

***Response to Arguments***

Applicant's arguments filed on Jan. 20, 2006 have been fully considered but they are not persuasive. for the following reasons :

Applicants' first contention that the applied (Shimoji or Mattox) references do not show or suggest making an integrated circuit "wherein the integrated circuit has a uniform thickness throughout the full extent thereof" is not persuasive because as stated above wherein the integrated circuit has a uniform thickness throughout the full extent thereof was not described in the specification as originally filed and therefore constitutes new matter and therefore the amendment has not been entered and therefore the limitations are not given patentable weight.

Therefore this alleged limitation cannot form the basis of distinguishing the claims from the applied prior art.

Applicants' next contention is that the applied (Shimoji or Mattox) references do not describe /suggest making an integrated circuit "wherein the integrated circuit is elastic while retaining its structural integrity" is not persuasive because Shimoji Fig. 6 B

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# 8, col. 4 lines 50-57 ( as stated in the rejection above) , col.5 lines 1-5 and lines 27-29  
( reproduced below)

~~bottom recessed parts 8. The resulting semiconductor device, therefore, has a sufficient strength and an excellent durability.~~

show that applicants' arguments are based on incomplete reading of the applied references and a complete reading shows the applied references showing teachings of making an integrated circuit "wherein the integrated circuit is elastic while retaining its structural integrity.

Therefore all of applicants' arguments are not found to be persuasive and all the pending claims finally rejected.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

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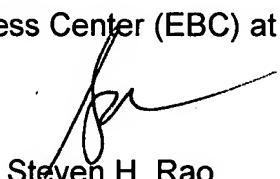
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is ( 571)272-1718. The examiner can normally be reached on 8.00 to 5.00.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

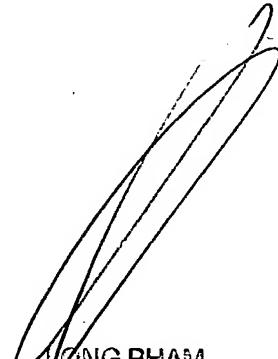
For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Steven H. Rao

Patent Examiner

March 29, 2006.



LONG PHAM  
PRIMARY EXAMINER